Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (currently amended) A memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective devices for receiving memory access requests;

a memory interface, for connection to a memory device; and

control logic, for placing received memory access requests into a queue of memory access requests, wherein, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, the control logic calculates the number of required data bursts and a starting address for each burst, and places the respective memory access requests into the queue of memory access requests such that back-to-back SDRAM read bursts can be performed, wherein the control logic determines whether the read access request is for data that can be delivered in a single burst of data, or for data that requires multiple bursts of data.

Claim 2. (original) A memory controller as claimed in claim 1, wherein, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, the calculated starting address for a first of said required data bursts comprises a row address and a column address, and the calculated starting address for a second and any subsequent required data bursts comprises a column address but no row address.

Claim 3. (original) A memory controller as claimed in claim 2, wherein the calculated starting address for the first of said required data bursts further comprises a chip select indication.

Claim 4. (original) A memory controller as claimed in claim 1, comprising a plurality of bus interfaces, wherein memory access requests received from different bus interfaces may be placed into the queue of memory access requests with different priorities.

Claim 5. (original) A memory controller as claimed in claim 1, comprising a plurality of bus interfaces, wherein memory access requests received from different bus interfaces may be placed into the queue of memory access requests with priorities determined in such a way as to maximise efficient usage of a memory bus connected to the memory interface.

Claim 6. (currently amended) In a memory controller, comprising at least one bus interface, each bus interface being for connection to at east one respective devices for receiving memory access requests; and a memory interface, for connection to a memory device; the method comprising:

determining from a memory access request if the memory access request requires a single burst of data, or multiple bursts of data to be read from the memory device;

when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, calculating the number of required data bursts and a starting address for each burst, and

placing the respective memory access requests into a queue of memory access requests such that back-to-back SDRAM read bursts can be performed.

Claim 7. (original) A method as claimed in claim 6, comprising, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, calculating said starting address for a first of said required data bursts comprising a row address and a column address, and calculating said starting address for a second and any subsequent required data bursts comprising a column address but no row address.

Claim 8. (original) A method as claimed in claim 7, comprising calculating said starting address for the first of said required data bursts comprising a chip select indication.

Claim 9. (original) A method as claimed in claim 6, in a memory controller comprising a plurality of bus interfaces, comprising

placing memory access requests received from different bus interfaces into the queue of memory access requests with different priorities.

Claim 10. (original) A method as claimed in claim 6, in a memory controller comprising a plurality of bus interfaces, comprising placing memory access requests received from different bus interfaces into the queue of memory access requests with priorities determined in such a way as to maximise efficient usage of a memory bus connected to the memory interface.

Claim 11. (currently amended) A memory controller, comprising:

at least one first bus interface, for connection to a master device for receiving memory access requests and for transmitting data to the master device;

a second bus interface, for connection to a memory device, such that data can be retrieved from the memory device in data bursts;

control logic, for receiving memory access requests from the ~~or each~~ first bus interface, and for calculating a required number of data bursts needed to deal with each received memory access request, and for determining if the memory access requests require a single data burst or multiple data bursts; and

a queue store, for storing data relating to required data bursts,

wherein the control logic stores data in the queue store, relating to each of the required number of data bursts.

Claim 12. (original) A memory controller as claimed in claim 11, wherein the control logic stores data in the queue store, relating to each of the required number of data bursts, such that the data bursts corresponding to a received memory access request can be retrieved without incurring a separate read latency for each data burst.

Claim 13. (original) A memory controller as claimed in claim 11, wherein the control logic stores data in the queue store, indicating that the required number of data bursts correspond to a single received memory access request.

Claim 14. (new) A memory controller as claimed in claim 11, wherein the control logic prioritizes the memory access requests based on bus interface type, or single burst, or multiple burst.

Claim 15. (new) A memory controller as claimed in claim 11, wherein the control logic determines from the memory access requests a burst length or a burst type.

Claim 16. (new) A memory controller as claimed in claim 1, wherein the multiple bursts of data are provided within one successive clock cycle.

Claim 17. (new) A memory controller as claimed in claim 1, wherein control logic determines if the read access requires a incrementing burst type of wrapping burst type.

Claim 18. (new) A memory controller as claimed in claim 1, wherein when a multiple bursts of data are required, after a first data burst, a starting address for subsequent data bursts are derived from the column address values for each of the subsequent bursts.

Claim 19. (new) A method as claimed in claim 6, wherein placing the respective memory access requests into the queue comprises queuing the memory access requests that require multiple bursts together so read latency is incurred only once.

Claim 20. (new) A method as claimed in claim 6, wherein determining comprises determining the burst length or the burst type.